Characterization of Ti/TiN and TiN Conductive Layer for High Temperature MEMS Devices

Peter Lange[1], Birger Ohlsen[2], Sebastian Puls[1] and Joerg Syre[1]
[1]Fraunhofer Institut fuer Siliziumtechnologie, Fraunhofer Str.1, 25524 Itzehoe, Germany
[2]FH Westkueste, Fritz-Thiedemann-Ring 20, 25746 Heide, Germany

ABSTRACT

The effects of temperature on micro heaters made of Ti/TiN stacks and pure TiN layers on bulk micromachined membranes have been studied. Ti/TiN stacks show a thermal stability up to 380°C, beyond that temperature an enhanced interaction within the stack and/or with adjacend layers leads to a degradation of the resistance. The pure TiN layers withstand temperatures up to 600 °C, this limitation is only given by the mechanical stability of the membran stack, which is destroyed beyond this temperature. These layers are suitable for sensors in which an elevated temperature provided by heating lines on a membran for thermal isolation and fast response is necessary for functionality.

INTRODUCTION

New conductive layer for heating and sensing in MEMS (Microelectromechanical System) devices operated at elevated temperatures are reported. These micro heaters are formed on membranes for fast response and thermal isolation to the chip frame. In applications such as calorimetric and anemometric flow sensors, gas sensors, thermopiles and IR sources the resistors are heated by a current flow. Thereby they have to withstand temperatures of several hundreds degree of Celsius. Degradation effects in the resistors have to be prevented, otherwise the external/internal signal conditioning circuit could not work properly. The fabrication of such devices in conjunction with standard CMOS processes shows considerable advantages as monolithic integration, low cost production and short cycle times. A variety of metals like Cr, Au or Pt are applied up to now in MEMS devices for this purpose. However, they are exhibiting the disadvantage of being mostly not compatible to IC processing [1]. In this respect polysilicon is the most applied material [2,3], but shows some altering behaviour at elevated temperatures. The refractory metals, for example Ta, W, Ti, are also providing candidates for this purpose. But many of these materials are highly reactive at elevated temperatures or show other drawbacks, for example a complicated process management, so the possibilities of choice are rather limited. Ti and TiN thin films are state of the art technology in MOS devices as diffusion barrier between Si and Al or Cu [4]. Because of this proven compatibility with front end MOS technology we have investigated Ti/TiN layers and pure TiN layers for the application as heating and sensing elements. For the protection against interdiffusion/oxidation effects the Ti thin films were covered with thin TiN layers.

EXPERIMENTAL

All experiments were carried out in a conventional MOS line on Si-wafers with <100> orientation and 150 mm in size. The Ti /TiN thin film consists of a sandwich of 25 nm TiN, 650 nm Ti and 50 nm TiN. These layers and the pure TiN layers of 500 nm thickness were deposited

in a reactive sputtering process (poisoning mode) on a stack of $Si_3N_4/SiO_2/Si_3N_4$ with a total thickness of 1 µm. The contact pads were covered with Aluminum for bonding reasons. After structuring the film via lithography and anisotropic dry etch processes the resistor lines are meanderlike with lines and spaces of 5 µm (see figure 1). Subsequent a passivation layer of 1 µm thickness was deposited by a plasma enhanced chemical vapour deposition process (PECVD). The membranes were formed by KOH anisotropic wet etching from the backside of the wafer. The size of the membrane is 1.2 mm by 1.3 mm. A drawing of the cross-section is given in figure 2. With this design a good thermal isolation to the chip-frame and a fast thermal response is assured.

The temperature coefficient (TC), the resistivity and the response to elevated temperatures were examined. The TC of these materials was measured on a wafer prober with a heatable „hot-chuck“ and compared later on with a measurement in a climate chamber. Within the measurement accuracy no significant deviations were observed. Additional measurements for the high temperature range have been performed using an IR imaging system. The resistivities were calculated from the measured sheet resistances using a conventional 4-point prober.

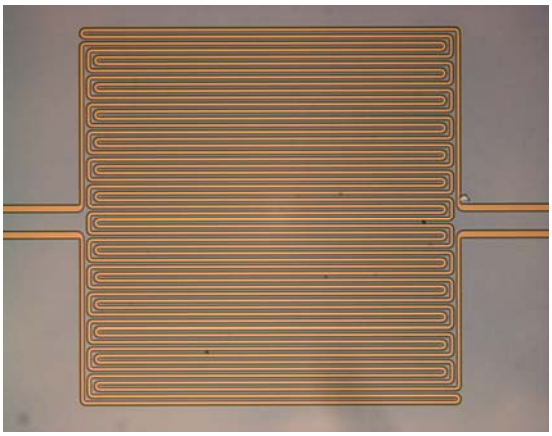


Figure 1. Meander structure of two resistance lines with 5 µm lines and spaces on a thin membrane.

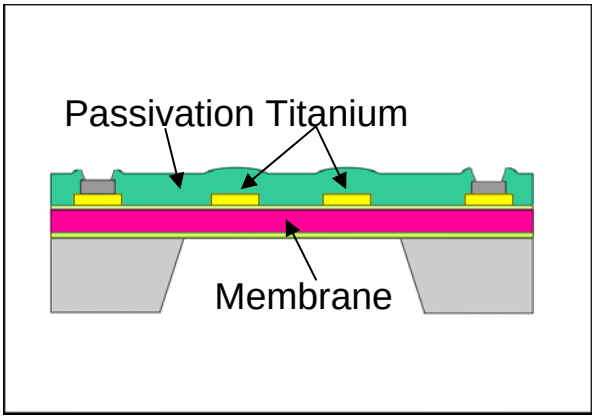


Figure 2. Cross-section of the membrane.

Temperature stress

The desired temperatures were adjusted by a current flow through the heating resistances. Thereby a voltage was imposed and continuously increased up to a maximum and decreased back to the starting value. This was measured with a parameter analyser and is shown examplarily in Figure 5, where the endpoint of the imposed voltage is stepwise increased from 21 to 30V.

The temperature was estimated in a first approximation by extrapolating the linear dependence of the TC.

This calculation from electrical data is only allowed if two aspects are considered:

- a material degradation (or any change in the materials structure) as effected by the imposed temperature.

This can be excluded, if the resistance remains constant

- after several high temperature cycles up to the same maximum value
- after continuous current stress at the reversible maximum voltage.

- a linear behaviour of the TC over a wide range of temperatures. The resistance-temperature dependence could only be measured until 240°C, because of experimental limitations of the hot chuck prober. A linear extrapolation beyond this range can be questionary.

Therefore additional measurements have been done by thermography using an infrared imaging system. This system is equipped with a scanner head and an optical telescope, which makes it possible to observe small areas with high resolution. The direct measurement of the temperature by thermography is difficult because of the unknown emissivity of the chip, respectively the chip surface. The following experimental set up has been used to measure the emissivity. Thereby the chip was mounted on a large iron block, which could be heated up to 700°C. A fully processed chip without membrane etching has been chosen. The reason was an assurement of a good thermal conductivity between the heater block and the chip. The temperature of the iron block has been measured with a thermocouple and the thermal image of the membran area with the resistance lines has been adjusted to this value under variation of the emissivity. We received values for the emissivity between 0.5 and 0.65 for a temperature range of 300°C to 600°C as is shown in figure 3.

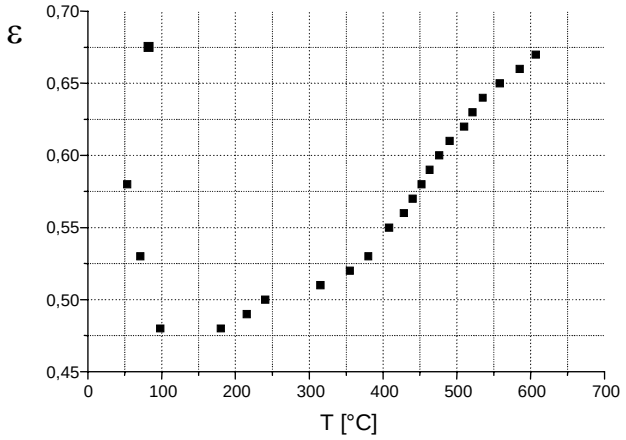


Figure 3. Emissivity ε as a function of temperature of a chip mounted on a heating block. The chip was completely processed except membrane etching to assure a good heatconductance.

RESULTS AND DISCUSSION

The Ti/TiN stack

The temperature dependence of the resistance R is shown in figure 4. The temperature covers a range from 30°C to 240°C and shows an extremly linear dependence with a correlation factor higher than 0.99. The TC (α) was calculated from such a measurement according to equation 1.

$R(T) = R(T_0) * (1 + \alpha(T - T_0))$ (1)
R = resistance (or any physical property), T = temperature, T_0 = reference temperature
α = temperature coefficient (TC) in the temperature range $\Delta T = T - T_0$; α is given in 1/K or K^{-1}.

For the Ti/TiN stack a value of 3830 ppm/K (22 - 240°C) was measured. This agrees well with reported data of 3800 ppm/K [5] given for the range of 0 -100°C. The resistivity was

measured with 44 μΩcm and fits also to reported data in the range of 40 to 54 μΩcm [5,6]. So far these properties of thin film Ti reveal no significant difference from those of bulk Ti.

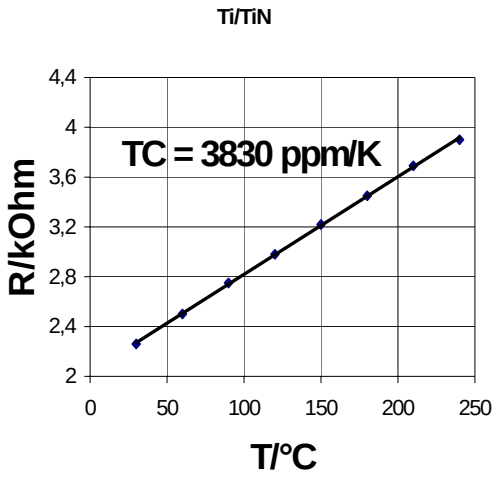


Figure 4. TC measurement of a Ti/TiN resistance.

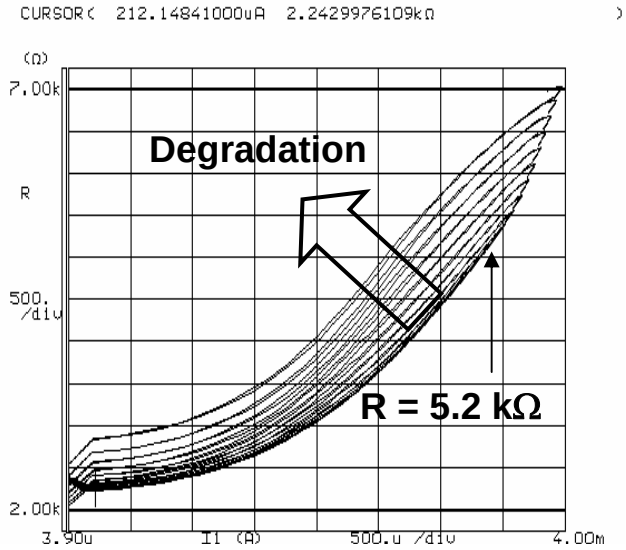


Figure 5. (right) Resistance characteristic (R/Ω vs I/A) for the Ti/TiN lines. The endpoint of the imposed voltage is stepwise increased from 21 to 30 V. The scaling on the I-axis is from 3.9 μA to 4.0 mA. Reversibility is given until R = 5.2 kΩ according to T = 380°C.

Performing the temperature stress experiments we achieved a highest temperature of 380°C under reversible conditions. This value corresponds to 5.2 kOhm and was calculated using the TC value from the above mentioned measurement extrapolating linearely from the lower (22 - 240°C) to the upper temperature range (T > 300°C). Also a 24 h current-stress at this temperature has not changed the value of the resistance. Above 380°C a distinct degradation of the resistance could be observed (see figure 5). The initial resistance has changed after the sweep cycle. This change is increasing with increasing voltage. Then also a change in the TC occured. This is a clear indication for a material transformation in the Ti/TiN layer.

The temperature of the resistance lines was confirmed independently by the thermographic method. Thereby the resistance lines were internally heated through a current flow to a value of 5.2 kΩ according to the calculated temperature of 380°C. The emissivities ε(T) of the chip were measured by the method described above. By using these emissivities we measured the temperature of the resistance lines with 398°C. However, internal heating produces a strong temperature gradient from the center of the heater area to the edge. Therefore the mean temperature of 398°C (AVG in figure 6) is an integrated value over the whole membran. The temperature in the center temperature exceeds 526°C and goes down to 238°C beyond the edges of the membrane. This is a consequence of the geometrical size of the heating lines (see figure 1). Within this limitation a good agreement between both methods of temperature measurement was obtained. In consequence this also true for the measured resistance, which appears as a mean value. We have calculated the TC again, the result is given in figure 7 with an TC value of 3774 ppm/K. Considering that the temperatures are means, the agreement with the low temperature TC is convincing. This result clearly shows the

appropriateness of a linear extrapolation beyond the initially measured temperatur range for this material.

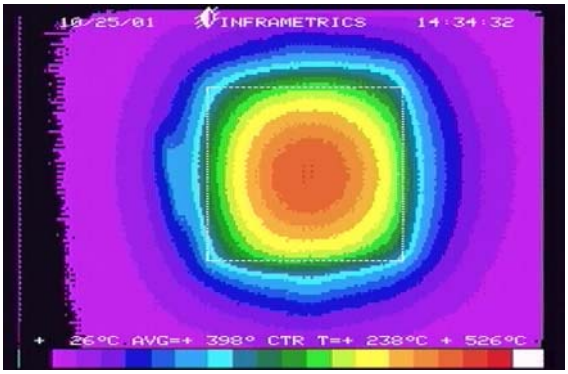


Figure 6. Infrared image of the membrane (area between the dashed lines), internally heated. The mean temperature of 398°C is an integrated value over all areas with different temperatures.

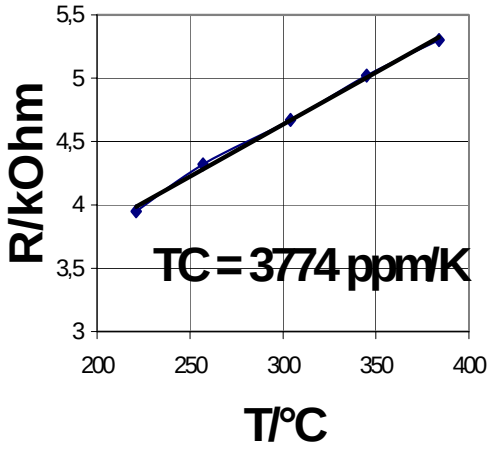
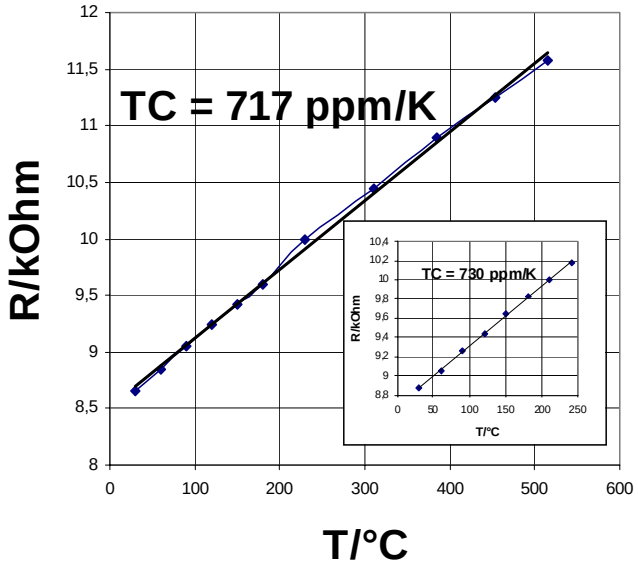


Figure 7. Measurement of the temperature coefficient TC by external heating of the chip.

The TiN layer

The temperature dependence of the resistance R for the TiN layer with 500 nm thickness measured on the „hot chuck“ is shown in the inlet of figure 8. Again, the temperature covers a range from 30°C to 240°C and shows also an extremly linear dependence with a correlation factor higher than 0.99. The TC of this layer was calculated with 730 ppm/K and is reported the first time. The resistivity was measured with 115 μΩcm in agreement with [4]. Temperature stress was possible until 600°C, at higher temperatures a degradation in the passivation layer occured. This is attributed to a different distribution of the mechanical stress in this stack compared to the above mentioned Ti/TiN stack, which contains a large amount of Titanium. This is supposed to attribute to a stress relaxation in the stack. A hysteresis was never observed (see figure 9).

The calculated temperature from interpolating the linear dependence of the TC has been verified again by thermography measurements. The chip was heated externally up to that point when the resistors reached 12 kOhm. The IR image together with the corresponding emissivities revealed a value of about 600°C for this resistance. These values have been estimated under the above mentioned limitations, so the reported data of the resistance and temperature are means. The TC (717 ppm/K) calculated from the whole temperature range (the internal heating from 30 - 180°C and the external heating from 230 - 520°C) shows no significant deviation from those calculated from the lower temperature range (730 ppm/K). The overall agreement is excellent considering the limitations in the accuracy of the high temperature determination. Thus it can be concluded, that for TiN it is also appropriate to extrapolate the linear behaviour of R(T) beyond the lower temperature range. However, so far the membran was undestroyed, even higher temperatures up to 800°C have been observed, without a change in the initial resistance at room temperature after switching off the heating current.



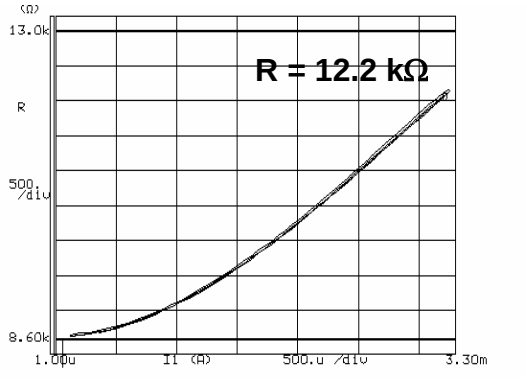


Figure 9. Resistance characteristic (R/Ω vs I/A) for the TiN lines. Reversibility is given until R = 12.2 kΩ according to T = 600°C.

Figure 8. Calculation of the TC of TiN from the temperature dependence of the resistance for internal heating (30°C - 180°C) and external heating (230°C - 520°C). In the inlet the calculation of the TC from internal heating (30°C - 240°C) only is shown.

CONCLUSION

Overall Ti and TiN show excellent characteristics. Both are compatible with CMOS technology and can easily be converted from standard processes. If a high TC is desired, the Ti/TiN stack can be selected for temperatures of max T = 380°C. This is usefull for sensor systems related to temperature measurements in moderate hot environments. For heating purpose only, the material of choice is the pure Titaniumnitride layer, since it withstands temperatures of at least 600°C without material degradation. For a practical application, however, a redesign of the geometrical shape of the resistance lines has to be done, so that no (or a negligible) temperature gradient appears. Also, a linear dependence of the TC from temperature over a wide range of temperatures has been shown for Ti/TiN and TiN.

ACKNOWLEDGEMENT

The support by the engineering team at the Vishay wafer fab at Itzehoe is greatfully acknowledged.

REFERENCES

[1] Gwiy-Sang Chung, Sensors and Actuators **A 112**, 55 (2004)
[2] N. Najafi, K.D, Wise and J. W. Schwank, *IEEE Trans. on Electron Devices* **41,** 1770 (1994)
[3] T. Neda; K. Nakamura and T. Takumi, *Eurosensors IX, Digest of Technical Papers*, p. 548 (1995)
[4] S. Wang, I. Raaijmakers, B.J. Burrow, S. Suthar,S. Redkar and K. Kim, *J. Appl. Phys.* **68**, 5176 (1990)