

# Tim Westmore

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## AREAS OF EXPERTISE

- Fabrication, packaging, and characterization of MEMS devices and products
- Surface and materials analysis using electron spectroscopy (Auger and XPS/ESCA)
- Wafer fabrication processes including diffusion, implant, and thin film deposition
- Statistical process control and design of experiments

## WORK EXPERIENCE

**Staff Engineer**, Silicon Light Machines, Sunnyvale, CA May 2001 to April 2004, May 2005 to present  
General responsibilities include developing, implementing, and qualifying new processes and products; characterizing yield and reliability failures; and supporting company efforts in materials analysis. Silicon Light Machines designs and develops a MEMS diffraction grating with applications in lithography, display, printing, and telecommunications.

### *Accomplishments*

- Developed a process to eliminate the loss of selectivity in a XeF<sub>2</sub> release that results from excess silicon (patent application filed); the sawn-edge passivation process enables release of a singulated MEMS devices
- Developed and demonstrated release-first and release-in-package packaging process flows for an electro-optical device; both flows allow packaging of fragile MEMS structures
- Determined the root cause of reliability failures for a thin film stack and assisted in developing improvements to the structure; the analysis identified areas of improvement for a wafer-level membrane packaging structure for RF devices
- Determined activation energy for operating stability in a Grating Light Valve; the results led to confirmation of surface charge carriers as a cause of unwanted changes in operating voltage
- Introduced an acceleration scheme to measure hillock and void formation in a MEMS structure created by a thermal gradient; the approach improves lifetime testing capabilities
- Analyzed the nitridization of titanium films in the development of conductive structures that enable stable operating voltages for a MEMS diffraction grating
- Qualified and implemented an improved glass cover brazing process, for wafer-level packaging, that eliminated glass cracks and a significant reliability concern
- Performed root cause failure analysis and implemented corrective action to solve a wafer-level hermetic solder seal failure; the solution played a significant role in allowing the company to complete development of a dynamic gain equalizer product

### *Current Projects*

- Project leader for developing a cavity package, including the assembly and backend processing; the new product and expands the company's applications base into UV lithography
- Project leader for implementing and qualifying a new device with increased light attenuation and reflectivity; encompasses process development, optical characterization, and reliability qualification; improvements increase throughput in customer computer-to-plate printing

**Materials Analyst**, Accurel, Sunnyvale, CA, March 1998 to April 2001

Responsible for providing contract materials analysis services on thin films, integrated circuits, and magnetic structures using AES, XPS/ESCA, AFM, and RBS; services provided for characterization or problem solving with written and verbal reports to customers; responsibilities also included developing customer relations and business strategies to increase group/company revenue

*Accomplishments*

- As manager of the surface analysis group, increased the group's annual revenue by more than 50% in less than two years, exceeding \$500K and surpassing projections

**Staff Engineer**, IBM Almaden Research Center, San Jose, California, May 1996 to March 1998

Sputter deposited GMR thin film structures for the development of non-volatile memory applications; analyzed materials and thin film structures using RBS, AES, XRD, XRF, and SEM; repaired and/or maintained analysis equipment including a high-energy ion accelerator and an x-ray diffractometer; research projects include inter-diffusion in copper nickel thin films to help understand reliability issues in magnetic head structures

**Process Engineer**, Genus, Sunnyvale, California, March 1995 to April 1996

Characterized and developed tungsten-silicide and tungsten-nitride thin film processes for the applications and technology development labs; qualified tungsten-silicide deposition processes at customer sites

**Process Engineer**, Integrated Device Technology, San Jose, CA, March 1992 to November 1994

Sustained diffusion, implant, and thin film wafer fabrication processes including PECVD dielectric films and LPCVD polysilicon/silicon nitride

**Process Engineer**, Teledyne Components, Mountain View, CA, January 1990 to July 1991

Sustained, improved, and/or developed diffusion and thin film wafer fabrication processes including diborane pre-deposition and PECVD nitride passivation; implemented computerized data collection for in-line measurements as part of an effort to improve manufacturing through statistical process control

**EDUCATION**

**BS, Materials Engineering**, Loughborough University of Technology, Leicestershire, UK, 1989

**MS, Materials Engineering**, San Jose State University, San Jose, California, 1997

**OTHER INTERESTS**

*Archeology* – expeditions on the colonial spice trade (Banda Neira, Indonesia); Paleo-Indian mineral mining (Mammoth Caves, Kentucky); Polynesian survival culture (Easter Island, Chile); and the development of the Iron Age Khmer Civilization (Ban Non Wat, Thailand)

*Teaching* – teaching a course titled Introduction to the Science and Engineering of Materials; an introductory lower division survey course on engineered materials; includes preparation of both course and lab work

*Marine Biology* - Captured identification photographs of whales for conservation efforts

*Photography*