

# Supradeep Narayana

## Research statement

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Over the past years, Moore's law of scaling in has enabled significant steps for improvements in computation and performance. But other technologies are fast catching up to either compete with silicon technologies or serve for better applications. Superconducting digital electronics, RSFQ (Rapid Single Flux Quantum) logic [1] in particular, is one of the fastest established technologies. RSFQ logic technology is based on Josephson junctions and data is represented in the RSFQ circuits by either the presence or sign of the magnetic flux quantum. ITRS, International roadmap on semiconductors [2, 3], in 2005 suggested that RSFQ logic as the most advanced technology close to replacing the existing CMOS technology. Superconducting electronics as name suggests, requires cooling the circuits to superconducting temperatures, typically to 4.2K. Superconducting technology is most beneficial in terms of high speed of operation and low power dissipation.

Apart from refrigeration- one of primary impediments to large scale development of superconducting electronics- some of the other difficulties for large scale integration area are: parasitic flux trapping, shielding, biasing of RSFQ circuits, low fabrication yield, and underdeveloped CAD tools. My research addressed issues dealing with large scale integration of superconducting circuits including parasitic flux trapping, low power consumption and multi-chip modules.

### Previous Research summary

After obtaining my bachelor's degree in electrical engineering from IIT Madras, I decided to pursue my doctoral studies in VLSI devices. After pursuing research in systems-on-chip in my 1<sup>st</sup> year of graduate study, I became more interested with emerging technologies. I moved to RSFQ laboratory to continue research in superconducting electronics under the guidance of Prof. Vasili Semenov. I was fortunate to gain experience in the complete design cycle, "from concept to testing", of a technology in the course of my doctoral research.

### 1. Flux trapping

In the beginning of my graduate research, I focused my efforts to study the effects of parasitic flux trapping in RSFQ circuits. When superconducting circuits are cooled, they trap flux- non superconducting vortices are formed in the superconducting films- destroying the functioning of the circuit or reducing the operating margins significantly. The probability of parasitic flux trapping increases linearly with the presence of magnetic field during cooling.

We developed a new model for characterizing interaction of vortices with RSFQ circuit elements. We also developed a new experimental methodology to measure the effects of flux trapping in the RSFQ circuits. The test circuits for the purpose were designed with in-house developed library cells. The experiments were carried out in both liquid helium Dewars and helium Cryo-coolers [4]. The measurement procedures developed were also able to characterize fabrication yield and fabrication spread. With our method also enables us to uniquely locate fabrication defects [5, 8].

Reducing the effects of parasitic flux trapping has always been a challenge in superconducting circuits. One method is to design holes in the ground planes called moats. The moats trap vortices, which help protect the RSFQ circuit elements from being damaged. A methodology was developed to systematically construct moats in RSFQ cells. With the newly designed moats in our RSFQ cells, we were able to eliminate the parasitic flux trapping for magnetic field for up to 20mG, which are five times higher tolerant to parasitic flux trapping than previously achieved[6].

### 2. Minimization of Power dissipation in RSFQ circuits

RSFQ circuits, with Josephson junction as active elements, are current biased. When large circuits are designed, the current value needed for biasing the entire circuit could be as high as 1A. This value of current is very large and this adds to the huge heat load. The large value of current bias in the designs leads to larger power dissipation than normally accepted. The large bias currents also create magnetic fields in various parts of the chips that can reduce the operating margins of the circuits, as RSFQ circuits are sensitive to magnetic fields. To overcome the problems due to the large bias current:

1. We developed a new logic family called the power independent RSFQ logic. The RSFQ cells have a memory element incorporated- a single junction squid which does not dissipate energy, when circulating current is lower than critical current - that preserves the state of the computation when bias is switched off. The circuit bias has to be switched only when we need to operate it and the rest of the time the bias can be switched off without disturbing the state of the logic. The power independence logic to design serial shift registers. The shift registers operated with nearly 20% margins [7, 9].

2. Superconducting currents are not dissipated in circuit components therefore we can “recycle” the applied bias current to one of the parts of the circuit. Current recycling is achieved by serial biasing of parts of a circuit using either capacitive or inductive coupling. The operation of the digital circuits up-to 1k junctions were demonstrated with large operating margins. The drawback of the circuits was they were sensitive to external magnetic field [5].

### **3. Multi-chip Module**

It has been demonstrated over the years, in superconducting electronic circuits, that the digital data transfer can exceed over several hundred giga-hertz in a single chip. However, in the process of designing large systems- which could encompass more than a single chip - a multi-chip module (MCM) approach is most suitable. In the MCM process two or more chips are bonded with different techniques such as adhesive bonding or soldering. The chips have specially designed bumps, connected with micro-strip lines for data transfer, for the bonding. This concept is not new, but we were able to develop a new bump structure that decreases the parasitic of the bump thereby increasing the cut-off frequency. In order to maximize the performance of MCM systems also developed a new bonding mechanism which has lower number of steps and this increases the probability of higher yield. We were able to successfully demonstrate the digital data transfer to exceed 109 GHz in the framework of 4.5KA/cm<sup>2</sup> Hypres fabrication. It is one of the fastest data transfer reported in the field of superconductor digital circuits with MCM's [10].

### **Present Research**

#### **1. Oversampling superconducting ADC**

The digital Transceiver, recently demonstrated by Hypres Inc., is one of the most complex superconducting circuit systems. An integral part of the Transceiver is the oversampling delta ADC. To improve the performance of the current ADC used, we are developing a low noise low pass oversampling ADC. The first step is to design a new high sensitive input transformer with a low pass filter, to reject the out-of-band noise. The low noise ADC is expected to have higher dynamic range. A model is being developed to evaluate the effects of clock jitter; noise by DC powered bias lines on the performance of the ADC. For greater accuracy the properties of the coil will be extracted by cryogenic measurements. The transformer has already been designed and submitted for fabrication. We expect to submit the complete front-end of the oversampling ADC for fabrication shortly.

#### **2. Multi-chip Module**

We have achieved significant progress in the area of MCMs. We believe that the performance of the test circuits were the main reason for the frequency limits of the data transfer. We are in the process of improving the circuit designs to obtain higher data transfer than previously achieved. Also the hard limit of the frequency cut-off limit for the bumps has not been established, so we are also designing circuits to measure the limits frequency cut-off the bumps.

#### **3. Magnetic sensors**

With ambient magnetic field being one of the major obstacles, for the RSFQ circuit functioning, shielding of the circuits is very critical. The process of developing a new shielding method: to nullify the already present residual magnetic field by applying enough counter field. Active shielding employs SQIFs (superconducting quantum interference filters), highly sensitive magnetic sensors capable of measuring with micro-gauss field accuracy, to determine the remnant magnetic field. Experiments are currently being carried out with newly designed SQIFs and shields.

### **Future directions**

With no present available technology taking over CMOS technology, which is believed now to be coming to the end of its journey, I think the approach of the future technologies will be: “best of all worlds”. Hybrid technologies are coming into prominence with progress emerging areas of NEMS, Spin transfer technologies and micro-fluids. We are already seeing MRAMs and NEMS successfully integrated into signal processing and sensors. In the future, hybrid systems are only going to grow, because it has come to considerable acceptance in the technology industry that one device technology cannot satisfy all the growing demands in computation, instrumentation and sensors.

Extensive studies are presently on going in the areas of NEMS, spin transfer techniques, micro fluids etc, but still fundamentals issues remain to be resolved for commercialization and exploiting their full potential. The fundamental issues revolve around the issues of fabrication, operating margins, device modeling, integration, etc. With my knowledge acquired in the area of device physics, circuit design and modeling, I am qualified to aggressively push for improving the current devices and exploring new possibilities for their applications.

I also believe that there is a need for a new design paradigm for devices/circuit design technology optimized for applications.

As a result I plan to work towards a new integrated device methodology for emerging technologies. I also believe that newly designed devices will require new innovative measurement procedures and methods for accurate characterization of the devices. I have independently taken the task of modeling spin-transfer device memory for integration with RSFQ devices. The high density current biased memory are very convenient features for current biased RSFQ circuits which are prominent for high speed and low power [12] .

To conclude, in the course of my research, I have been in the development of the methods that will solve a few of the problems facing the superconducting digital circuits for large scale integration. In the future, I am interested in pursuing research in similar areas of emerging technologies that could hasten the development of new products. I believe that the situation most beneficial for me will to involve myself in new, underdeveloped and emerging technologies, requiring a certain degree of innovation, modeling and experimentation. I believe that my experience in research work, which has been performed with a new of colleagues in both academia and industry, has equipped to take on new adventures. I am excited at the prospect of learning and contributing to make an impact.

#### References

1. K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction digital technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.* 1, 3 (1991).
2. The International Technology Roadmap for Semiconductors, 2005 version.
3. NSA assessment report on RSFQ, 2005.
4. Yuri Polyakov, Supradeep Narayana and V.K. Semenov, "Flux trapping in superconducting RSFQ circuits", *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, June 2007.
5. Supradeep Narayana and V.K. Semenov, "RSFQ circuits in magnetic field," *IEEE Appl. Supercond.*, at ASC 2008.
6. Supradeep Narayana, Yuri Polyakov and V.K. Semenov, "Evaluation of flux trapping superconducting circuits," accepted for publication in *IEEE Appl. Supercond.*, 2009.
7. Supradeep Narayana and V.K. Semenov, "Power Independent RSFQ logic circuits," *proceeding of 12th ISEC 2007*, Washington, pp. 1-4.
8. Supradeep Narayana and V.K. Semenov, "Comparison of flux trapping in power independent and RSFQ D flip-flops", *15th US workshop in Superconducting devices and circuits*, 2007.
9. Supradeep Narayana, D. Averin and V.K. Semenov, "Power minimization techniques in RSFQ circuits," submitted to *Supercond. Sci and Tech.*, Institute of Physics.
10. S.K. Tolpygo, D.A. Tolpygo S. Narayana, V.K. Semenov, R.T. Hunt, "Wafer bumping process and inter-chip connections for ultra-high data transfer rates over 100GHz in multi-chip modules with superconductor integrated circuits," accepted for publication in *IEEE Appl. Supercond.*, 2009.
11. Hypres design rules, available online in [www.hypres.com](http://www.hypres.com)
12. Supradeep Narayana, "Feasibility of MRAM-SRFQ systems," manuscript in preparation.