MONA JOSHI

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SUMMARY

A Process Engineer in a Fortune100 semiconductor industry with 4 years of experience in Ion Implantation and Chemical Mechanical Planarization (CMP) with particular emphasis on Capacity Improvement, Cost Reduction, Yield Enhancement, Quality control, Product Optimization, Process development and Cycle time reduction all based on Lean Management principles. Strengths include project management, effectively working with cross–functional and cross location teams, troubleshooting and ability to learn quickly. A reliable team member with ability to work independently, self-drivingly, and in an extremely organized fashion.

TECHNICAL SKILLS

- Knowledge and Experience working in a Manufacturing Industry, particularly in Process Engineering in Chemical Mechanical Planarization (CMP) and Ion Implantation.
- Implementation of Process Control techniques using Statistical methods (SPC, DOE, FMEA) and analyzing data through Spotfire and JMP.
- Experience with End of line parametric / yield data analysis and ability to drive improvement actions.
- Knowledge of MEMS designing using L-edit.
- Knowledge of Chip Scale Packaging and Area Array Packaging.
- Knowledge of Semiconductor Device Physics.

PROFESSSIONAL EXPERIENCE

TEXAS INSTRUMENTS INC., DALLAS, TEXAS
A FORTUNE 100 COMPANY

- **Process Engineer Shallow Trench Isolation CMP** **2007 – Present**
  - Implemented pads at STI CMP that improved Yield by 2%. Tool utilization improved by 3%.
  - Implemented new slurry at STI CMP. A cost savings of 50 cents per wafer was noted.
  - Optimized the tool qualification strategy to prevent excursions
  - Active team member of the defect focus team driving solutions to eliminate defects causing yield loss at the end of line.
  - Lead Ad –hoc defect focus teams to resolve inline process issues induced as a result of process marginality.
  - Experience in working on AMAT Mira Polishers.
  - Daily sustaining using SPC, disposition material, update internal documentation, Standard Operating procedures and process specifications.
  - Provide training to engineering technicians, production associates.
- **Process Engineer Implant** **2005 - 2007**
  - Part of the engineering team responsible for a process transfer and release for an analog technology from Asia to USA.
  - Reduced cycle time by implementing a way to level the load and better utilize the tools via capacity improvement actions.
  - Module Pilot wafer champion focusing on reducing pilot costs by evaluating better alternatives without compromising quality.
  - Main focus was on clone tool releases and capacity improvement actions
  - 5S engineering module champion – worked on different activities that focused on the “Five S” Lean tools: Sort, Set, Shine, Standardize and Sustain.
  - Experience in working on Axcelis Implanters and Varian Implanters.

- Daily sustaining using SPC, disposition material, update internal documentation, Standard Operating procedures and process specifications.
- Provide training to engineering technicians, production associates.

UNIVERSITY OF TEXAS AT ARLINGTON, ARLINGTON, TEXAS

- **Student Assistant** **2004 -2005**
  - Main duties were to troubleshoot, research, diagnose, document and resolve issues relating to UTA computer resources that include handling incoming calls, processing Helpdesk emails and design of web pages. Recording client support using Front Range Solutions, HEAT support center software. Providing UNIX account support.

EDUCATION

Masters of Science (MS) (Electrical Engineering)	University of Texas at Arlington, USA	2003-2005
Bachelor of Science (BS) (Electronics and telecommunication)	University of Pune, India	1998-2002

RELEVANT GRADUATE COURSES

Semiconductor Device Theory
Introduction to MEMS
VHDL
Radio Frequency Circuit Design
Silicon IC Fabrication Technology
Advanced MEMS
Chip Scale and Area Array Packaging

CLEAN ROOM FABRICATION PROJECTS AND EXPERIENCE

- Parameter extraction for Deal-Grove Oxidation model – Performed wafer cleaning, growth of thermal oxide on the wafer, measured the thickness of the oxide at specific interval of time using the Ellipsometer, compared and analyzed the data to extract the coefficients for Deal-Grove oxidation model.
- Diffusion – Performed wafer cleaning, spin coating, diffusion and resistivity measurements using the four-point probe.
- Determine thickness of photo-resist layer as function of spin speed – Photo-resist was deposited on the wafer at different spin speeds. The resist thickness was measured using the Ellipsometer. Data was analyzed.
- Fabrication and characterization of MOS capacitor – Oxide of known thickness was grown on the Silicon wafer. The metal of known thickness was deposited on the oxide. Pattern was developed by Photolithography and Etching steps. The fabricated MOS capacitor was tested and characterized.

COMPUTER PROFICIENCY

- Circuit Analysis: PSPICE
- Data analysis software: SPOTFIRE, JMP
- Design and Simulation Tools: ModelSim, Precision, Xilinx, L-Edit
- Languages and Software: C Language, MATHCAD, MATLAB, Assembly Language

AFFILIATIONS

- Mentor for undergraduate / graduate students – MentorNet
- Active member in the United Way Campaign in Dallas
- Liaison for a Non-Profit Organization helping Patients – Guillian Barre Syndrome Foundation PA, USA.